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COMPLETED SOLUTION FOR RADIATION-HARDENED BMTI FPGA SYSTEM IN AEROSPACE APPLICATION

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The single event effects such as SEU/SET will cause dysfunction to FPGA which work in space radiation environment. This paper focuses on the SEU effects of SRAM-based FPGA and mitigation techniques. A completed solution based on radiation-hardened FPGA and intelligent scrubbing chips produced by Beijing Microelectronics Technology Institute (BMTI) is constructed. To evaluate effectiveness of the solution, a verification test is designed and heavy ion irradiation test is carried out.

Keywords: *FPGA, SEU, Intelligent Scrubbing.*

Introduction. Nowadays, Field Programmable Gate Array (FPGA) has been widely used in advanced weapon equipment system, such as missiles, rockets, satellites, spacecraft, aircraft and so on [1]. However, the exposed problem, that SRAM-based FPGA is susceptible to Single Event Effects (SEE), has caused wide attention of the FPGA research institutes and users. In order to ease the Single Event Upset (SEU) effects occurred in SRAM-based FPGA, such measures usually can be used. One way is to use the anti-SEU FPGA, such as anti-fuse FPGA product, but which can be limited in large scale application due to the embargo and price issues. The other way is to choose the anti-SEU SRAM-based FPGA. Another way is to apply the mitigation techniques to FPGA, such as configuration memory scrubbing technique [2–4], Triple Modular Redundancy (TMR) technique [5] and so on. Especially, the configuration memory scrubbing technique can avoid the system failure caused by SEU effects in theory. The SEU effects mitigation technique, in SRAM-based FPGA application, needs to analyze according to the development of the specific task. Xilinx provides a matrix analysis chart as a basis for selection, as shown in Fig 1.

This paper introduces a completed solution based on the SEE-hardened SRAM-based FPGA and general intelligent scrubbing control chip for long term on orbit spacecraft electronic system. Besides, the ground radiation verification experiment has been carried out to prove the effectiveness of the solution we proposed.

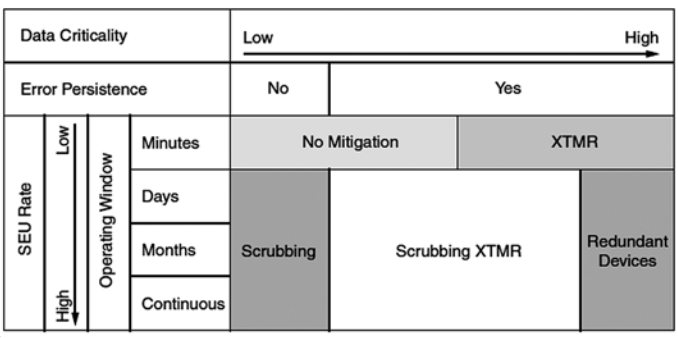

Fig. 1. **Mitigation Scheme Matrix**

System Solution Composition. The core of this solution is the 3,000,000 gates radiation-hardened SRAM-based FPGA (BQR2V3000) from BMTI. The FPGA is used to provide generic I/O, arithmetic and control functions. The general intelligent scrubbing control chip (BSV2) is used to provide FPGA with the timing scrubbing function. The configuration Programmable Read Only Memory (PROM) provides the configuration bitstream for FPGA.

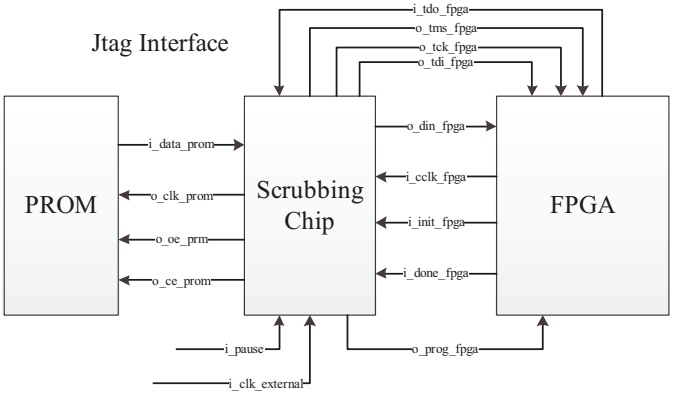

Fig. 2. **Schematic of the system**

The BSV2 can scrub the FPGA through the JTAG interface. Besides it also has the Master-Slave configuration function. The radiation resilience performance of the core devices is shown in Table 1.

Table 1. The radiation resilience performance of the core devices

Item	BQR2V3000	BSV2
TID	≥100 krad (Si)	≥100 krad (Si)
SEL	≥75 MeV·cm²/mg	≥75 MeV·cm²/mg
SEU	<5 MeV·cm²/mg	≥37 MeV·cm²/mg

Radiation Hardened SRAM-Based FPGA. The BQR2V3000 from BMTI is a high performance, high reliable SRAM-based FPGA. Its architecture is the same as the Virtex II series SRAM-based FPGA (XQR2V3000) [6] of Xilinx. The function and performance are compatible with XQR2V3000. Besides, it can be used with the 17 series configuration PROM

of Xilinx. And it supports JTAG, Serial, and parallel configuration modes. BQR2V3000 [7] uses island design architecture, and its functional unit is on the two dimension grid, connected by the horizontal and vertical wiring. BQR2V3000 contains various programmable resources, such as Configurable Logic Blocks (CLB), Input/output Blocks (IOB), and other IP resources as shown in Fig. 3

The leading-edge 0.13μm CMOS 8-layer metal process and the BQ2V architecture are optimized for high speed with low power consumption, with the densities of 3,000,000 system gates. The resources of BQR2V3000 are shown in Table 2, and the features are listed below:

- CLB resources include four slices and two 3-state buffers. Each slice is equivalent and contains: two function generators (F and G), two storage elements, arithmetic logic gates, fast carry look-ahead chain;
- The block SelectRAM memory resources are 18 Kb of dual-port RAM, programmable from 16K $\times$ 1 bit to 512 $\times$ 36 bits, in various depth and width configurations;
- The multiplier block is a dedicated 18 x 18-bit multiplier and is optimized for operations based on the block SelectRAM content on one port;
- Up to 12 DCM blocks are available. To generate deskewed internal or external clocks, each DCM can be used to eliminate clock distribution delay;
- IOBs are programmable and can be categorized as input block, output block and bidirectional block, and it supports large varieties of both single-ended and differential I/O standards.

General Intelligent Scrubbing Control Chip. BMTI is the first device producer carrying out the research on FPGA configuration memory scrubbing technique, who has been actively exploring the SEU effects mitigation and correction techniques of SRAM-based FPGA configuration memory [8]. The goal is to avoid the accumulation of SEU in the configuration memory caused by the circuit function failure, and not to affect the normal function of the FPGA circuit. With accumulated experience in radiation-hardened design, the BSV2 targeting SRAM-based FPGA has been designed. Because of the SEE problem in SRAM-based FPGA space application, BSV2 provides a real time scrubbing solution, which can significantly reduce the design complexity of the scrubbing system. This circuit supports the Xilinx Virtex II series radiation hardened FPGA such as XQR2V1000, XQR2V3000, XQR2V6000, and also supports BMTI BQR2V1000, BQR2V3000, BQR2V6000, which are compatible with Xilinx product features.

BSV2 uses synchronous circuit design, which would not affect the normal function of the FPGA scrubbed. Without power down, BSV2 can load the bitstream from the PROM into the configuration memory of FPGA. This chip recognizes the type of FPGA by readback and automatically sets the scrubbing parameter. By indentifying the feature words resides in bitsream,

Fig. 3. **The structure of BQR2V3000**

Table 2. The resources of BQR2V3000

Device	System Gates	CLB (1 CLB = 4 slices = Max 128 bits)			Multiplier Blocks	SelectRAM Blocks		DCMs	Max I/O Pads
		Array Row x Col.	Slices	Maximum Distributed RAM Kbits		18 Kbit Blocks	Max RAM (Kbits)		
BQR2V3000	3M	64 x 56	14,336	448	96	96	1,728	12	720

the non-configuration bitstream data, such as file name, device type and design date will be screened. The BRAM data can also be identified, avoiding users' data modified. The built-in error correction and recovery function can cut off the datapath immediately once error detected, and reset the FPGA configuration state machine through JTAG command. The structure of BSV2 is shown in Fig. 4.

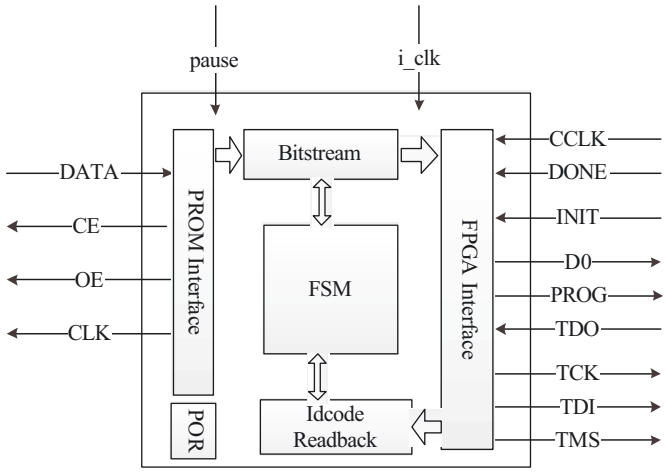

Fig. 4. **The structure of BSV2**

Ground Radiation Verification Experiment. A Software and hardware system platform [9] for ground radiation verification experiment is designed to prove the rationality and effectiveness of the solution we proposed. The ground radiation experiment has been carried out, utilizing the HI-13 tandem accelerator in China Institute of Atomic Energy and HIRFL cyclotron in Institute of Modern Physics, Chinese Academy of Sciences.

Hardware Platform. The hardware platform consists of two parts: a current collection board and a SEU effects radiation experimental board. The schematic of hardware platform is illustrated in Fig 5.

The current collection board provides the power supply for the SEU effects radiation experimental board, and monitors the core power supply and I/O power supply of the FPGA under test. The current collection board consists of five modules: a power supply interface for the control region of SEU effects radiation experimental board, a power supply interface for the experimental region, the power supply for the experimental region, a PC communication interface and the power supply for the current collection board.

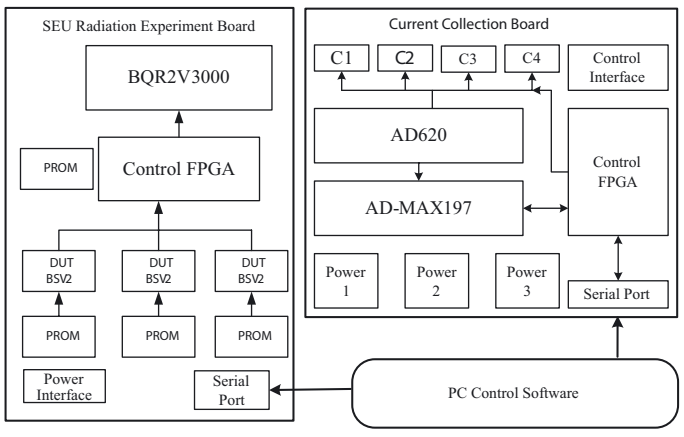

Fig. 5. **Schematic of hardware**

The SEU effects radiation experimental board consists of the scrubbing chip BSV2, a control FPGA and a FPGA under test. Before radiation period starts, the control FPGA connects BSV2 with FPGA under test. During the radiation period, the control FPGA monitors the scrubbing function of BSV2 to decide if the SEU happens, and uploads the function failure times of the FPGA under test back to PC terminal.

Software Platform. The PC software is the control center of the SEU effects radiation experimental system. As is illustrated in Fig. 6, the experimental system software consists of parameters setting, procedure control and data display.

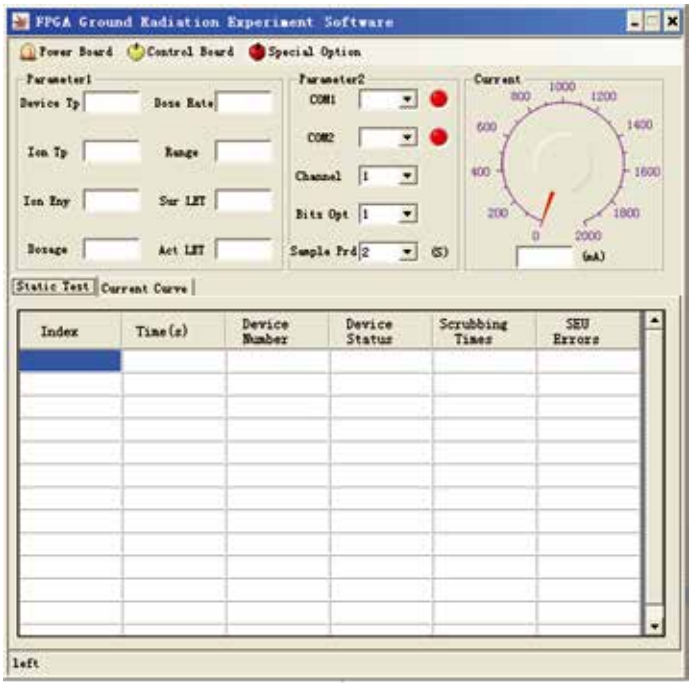

Fig. 6. **Software of the experiment system**

The experimental software possesses such functions as FPGA under test controlling, scrubbing function monitoring and latch-up monitoring. Before experiment starts, some parameters related to experimental information are need to be set, such as device type, heavy ion type, heavy ion energy, total dose, dose rate, range in silicon, surface LET and active LET; the parameters of two communication serial-ports, chip selection and sample period are also need to be set. During radiation period, the SEU effects radiation experimental board works first, then the working current of BSV2 and scrubbing function are monitored. According to the sample period, the numbers of SEU errors and scrubbing times are uploaded to PC terminal through serial-port at the same time.

Experimental Result. Large numbers of heavy ion radiation experiments are carried out to evaluate the impact of SEU effects, using the ground radiation experiment system we designed. The experimental results prove that it can reduce the SEU probability effectively and increase the system radiation-resilience performance greatly using BQR2V3000 FPGA and intelligent scrubbing chip BSV2 both together. With the completed SEU mitigation solutions used, radiation-hardened device and scrubbing technique typically, the space electrical equipments which include SRAM-based FPGA could work stably and continuously on orbit.

Conclusion. Through the research on SEU effects and mitigation techniques for space-used SRAM-based FPGA, a com-

pleted solution based on radiation-hardened FPGA and intelligent scrubbing chips produced by BMTI is constructed. The radiation experimental system is designed and the comprehensive experiment validation is carried out. The experimental results prove that the proposed solutions can effectively mitigate the impact of SEU effects for SRAM-based FPGA, and can be applied in the space radiation environment.

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КОМПЛЕКСНОЕ РАДИАЦИОННО-СТОЙКОЕ РЕШЕНИЕ ДЛЯ КОСМИЧЕСКОГО ПРИМЕНЕНИЯ НА ОСНОВЕ ПЛИС, РАЗРАБОТАННОЙ В BMTI

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Одиночные эффекты типа SEU/SET, проявляющиеся в условиях космического пространства, могут нарушить корректное функционирование ПЛИС. В статье рассмотрены программно-аппаратные методы повышения радиационной стойкости ПЛИС на базе статического ОЗУ. Пекинский институт микроэлектронных технологий (Beijing Microelectronics Technology Institute — BMTI) предлагает готовое решение на основе радиационно-стойкой ПЛИС и специального интеллектуального чипа, так называемого scrubbing chip, выполняющего функции проверки корректности кода микросхемы конфигурационной памяти. Для оценки эффективности применения этого решения была создана методика с использованием облучения тяжелыми заряженными частицами.

Ключевые слова: *FPGA, SEU, интеллектуальный чип.*

К 80-ЛЕТНЕМУ ЮБИЛЕЮ АНАТОЛИЯ МИХАЙЛОВИЧА СОМОВА

Уже более полувека не иссякает источник творческой энергии видного российского специалиста в области антенн профессора А.М. Сомова.

Анатолий Михайлович Сомов родился 1 августа 1935 г. в Барнауле. В 1960 г. окончил Казанский авиационный институт (ныне Казанский государственный технический университет им. А.Н. Туполева) по специальности «Радиотехника» и был направлен на работу в специальное конструкторское бюро Красноярского радиотехнического завода. Участвовал в освоении производства системы управления межконтинентальных баллистических ракет, разработал и внедрил в производство первые в стране серийные офсетные антенны с управляемой диаграммой направленности для малоканальных мобильных станций дальней тропосферной связи.

В 1966 г. А.М. Сомов стал сотрудником НИИ Радио. В 1967 г. он участвовал в разработке спутниковой системы «Орбита» для передачи телевидения в районы Дальнего Востока и Сибири, комплекса спутниковой связи для кораблей «Космонавт Юрий Гагарин» и «Академик Сергей Королев». В 1972 г. А.М. Сомов защитил кандидатскую диссертацию и в 1988 г.— диссертацию на соискание ученой степени доктора технических наук. В 1993 г. ему присваивается звание профессора.

С 2002 г. по настоящее время А.М. Сомов работает главным научным сотрудником НИИ Радио.

За добросовестную научную и педагогическую работу А.М. Сомов награжден орденом Трудового Красного Знамени, медалью ордена «За заслуги перед Отечеством» II-й степени, медалями «За трудовое отличие», «850 лет Москвы». Его труд отмечен знаками «Почетный радист», «Изобретатель СССР» и др.

Подробнее о жизненном пути А.М. Сомова см. *www.elsv.ru*.

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